ERRATA SHEET

7712
Dynamic RAM Card
USER'S MANUAL

IMPROVEMENTS

- Digital Filtering has been added to MCSYNC*.
- Dynamic RAM timing margins have improved.
- The 7712 meets all requirements of STD 8088 Specification version 1.1 for 8088-based timing at 5 MHz.

RESULTING COMPROMISES

- 8085 processor STD cards are no longer supported by the 7712 Dynamic RAM Card. The STD 8085 specification does not ensure timing that meets 7712 requirements.

- DMA controllers using 16-bit addressing are no longer supported by the 7712 because they do not supply MCSYNC*. Controllers using 20-bit addressing (such as the 7388A Floppy Disk Controller) will operate properly.

- The 7712 performs transparent refresh except during continuous, consecutive write operations (e.g., during the 8088 repeated string store instruction). The 7712 asserts WAITRQ* and performs the refresh.

CHANGES TO THE 7712 CONFIGURATION

- Because 16-bit DMA is no longer supported, W3 has the DMA register disabled by removal of all jumpers.

CHANGES TO THE 7712 USER'S MANUAL

- Please disregard all references throughout the manual that apply to operation with 8085 processor cards and 16-bit address DMA cards. Pages 3-7 through 3-14 refer to 8085 memory management and may also be disregarded.

  The entire Section 4 on operating software is based on 8085 programs. The flowcharts and discussions may be used for reference only.

- Page 1-1, PURPOSE, first paragraph:

  Delete the phrase "8085 (6.25 MHz)." Change "Pro-Log 7388" to "Pro-Log 7388A."

- Page 1-1, PURPOSE, last paragraph:

  Change "without wait states during all modes" to "without wait states during most modes."

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- Page 1-1, FEATURES:

  Change the first item to read "Compatible with 8088 (at 5 MHz) and 20-bit address DMA controllers."

- Page 2-5, Figure 2-3, jumper W3:

  Remove the asterisk (*) for jumper "1-2" and add an asterisk for "no jumper."

- Pages 2-9 through 2-12, Figures 2-7 through 2-10:

  Replace figures with attached figures 2-7A through 2-9B.

- Page 3-18, REFRESH, first sentence:

  Change "refresh circuit operation is completely transparent to the user" to "refresh circuit operation is transparent unless continuous, consecutive write operations occur."

- Page 3-18, Asynchronous:

  Delete the last sentence beginning "The WAITRQ* line ..."

- Page 3-18, next-to-last paragraph:

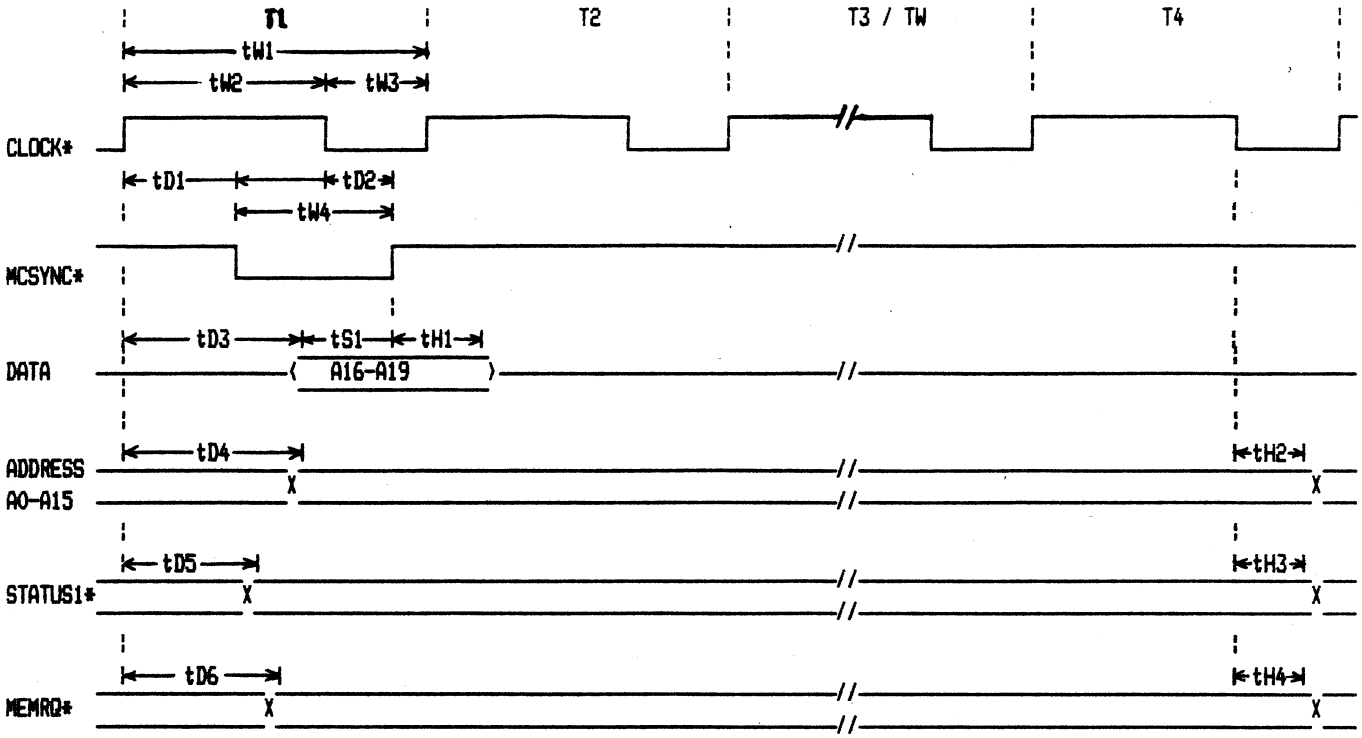
  Modify to read "The controller services the refresh (refresh enable is reset) at the end of the next read access cycle on the bus (typically less than 2 microseconds) in either the synchronous or forced modes. If there is no bus activity, or no read access cycles, refresh enable remains high and the refresh timer output goes low. This condition triggers an asynchronous refresh from the controller, the refresh enable latch is reset, and a wait cycle is requested."

- Page 3-18, last paragraph:

  Delete the phrase "or processor performance degradation."

- Page 3-19, DMA PROCESSOR COMPATIBILITY, HARDWARE:

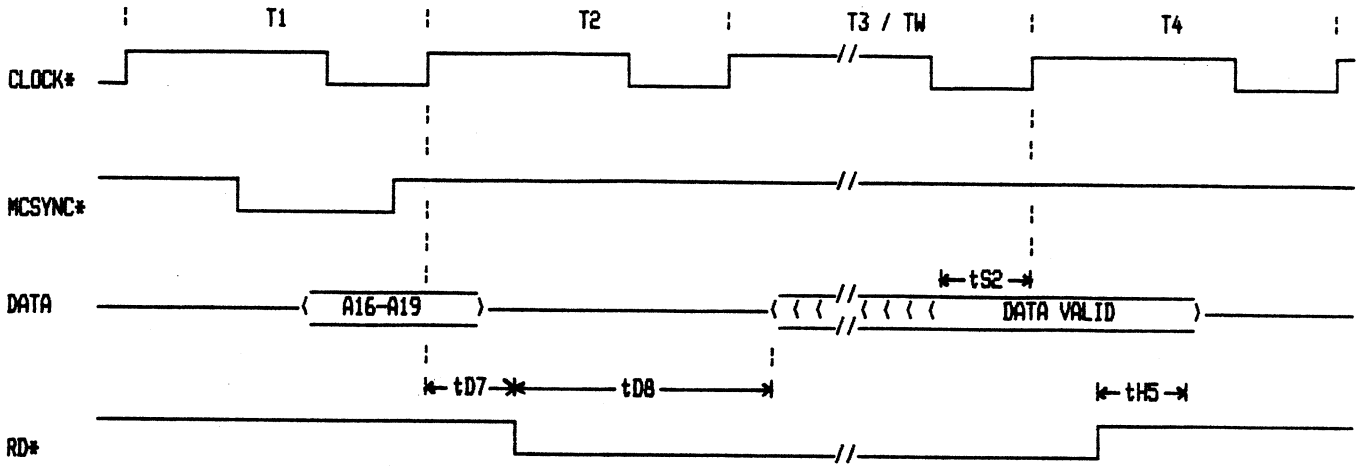
  Add MCSYNC* to the DMA processor signals. Remove the last sentence beginning "The most critical ..."



SYMBOL	PARAMETER	5.0 MHz MIN	5.0 MHz MAX
tD1	Delay from CLOCK* to MCSYNC* low	-10	
tD2	Delay from CLOCK* to MCSYNC* high		115
tD3	Delay from CLOCK* to Address A16-19		135
tD4	Delay from CLOCK* to Address A0-A15		170
tD5	Delay from CLOCK* to STATUS*		185
tD6	Delay from CLOCK* to MEMRQ*		170
tH1	Address 16-19 hold after MCSYNC*	17	
tH2	Address hold after CLOCK*	-50	
tH3	STATUS* hold after CLOCK*	-50	
tH4	MEMRQ* hold after CLOCK*	-50	
tS1	Address 16-19 setup to MCSYNC*	10	
tW1	CLOCK* width	199	6000
tW2	CLOCK* high width	110	
tW3	CLOCK* low width	60	
tW4	MCSYNC* pulse width	59	

All times given in nanoseconds.

Figure 2-7A. Bus Status and General CPU Timing (7712)

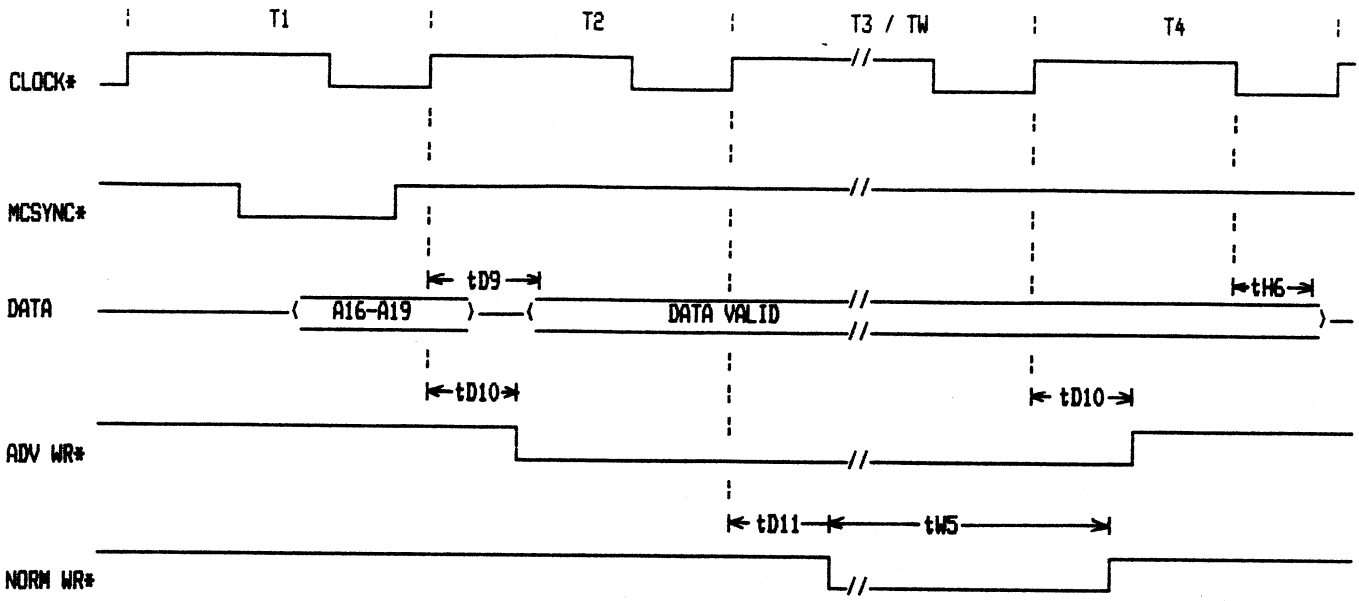


SYMBOL	PARAMETER	5.0 MHz MIN	5.0 MHz MAX
tD7	Delay from CLOCK* to RD* low	-50	190
tD8	Delay from RD* to Data driven on BUS	15	50
tH5	Data hold after RD*	15	50
tS2	Valid Data setup to CLOCK*	65	

All times given in nanoseconds.

Figure 2-7B. CPU Read Timing (7712)
(STATUS1* is available)

Note: The 7712 meets STD 8088 Specification version 1.1 without exception for 5 MHz 8088 STD cards.

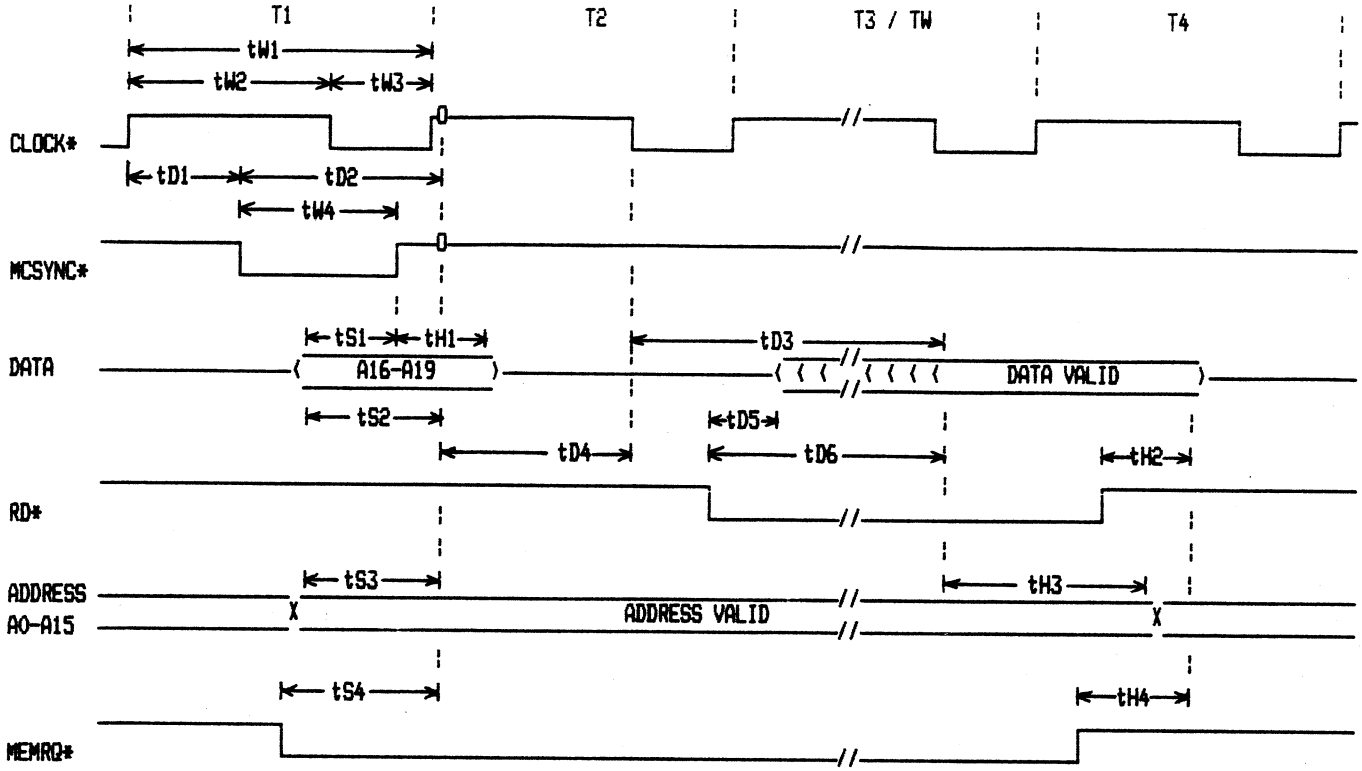


SYMBOL	PARAMETER	5.0 MHz MIN	5.0 MHz MAX
tD9	Delay from CLOCK* to Valid Data		145
tD10	Delay from CLOCK* to Advanced WR* low	-50	
tD10	Delay from CLOCK* to Advanced WR* high	-50	
tD11	Delay from CLOCK* to Normal WR* low		100
tH6	Data hold after CLOCK*	-50	
tW5	Normal WR* pulse width	85	

All times given in nanoseconds.

Figure 2-7C. CPU Write Timing (7712)

Note: The 7712 meets STD 8088 Specification version 1.1 Without exception for 5 MHz 8088 STD cards.



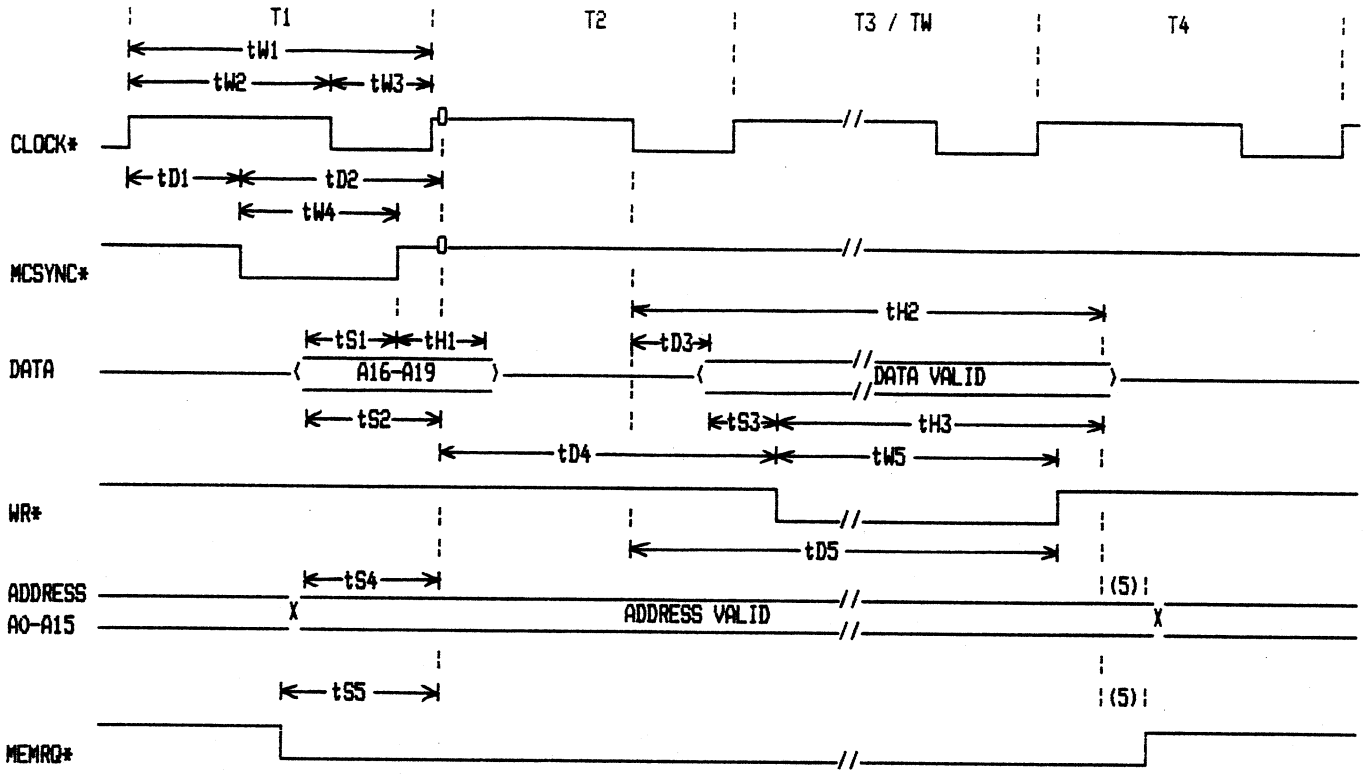
SYMBOL	PARAMETER	MIN	MAX
tD1	Delay from CLOCK* to MCSYNC* low	-10	
tD2	Delay from MCSYNC* to MCSYNC* and CLOCK* high	60	
tD3	Delay from CLOCK* to valid Data (tAR - see notes)		260
tD4	Delay from MCSYNC* and CLOCK* high to RD*	-50	
tD5	Delay from RD* to Data driven on BUS	15	50
tD6	Delay from RD* to valid Data (tAR - see notes)		205
tH1	Address 16-19 hold after MCSYNC*	17	
tH2	Data hold after RD*	15	50
tH3	Address 0-15 hold after Data valid	-50	
tH4	Data hold after MEMRQ*	15	60
tS1	Address 16-19 setup to MCSYNC* low	10	
tS2	Address 16-19 setup to MCSYNC* and CLOCK* high	60	
tS3	Address 0-15 setup to MCSYNC* and CLOCK* high	30	
tS4	MEMRQ* setup to MCSYNC* and CLOCK* high	25	
tW1	CLOCK* width	199	6000
tW2	CLOCK* high width	50	
tW3	CLOCK* low width	50	
tW4	MCSYNC* pulse width	35	

All times given in nanoseconds.

Notes:

1. Read access starts with CLOCK* going low in T2 regardless of RD*. Access will not complete until after RD*.
2. Worst case read access time (tAR) is based on tD3 or tD6; whichever causes the later access based on RD*.

Figure 2-8A. DMA Read Timing (7712)
(STATUS1* is not active)



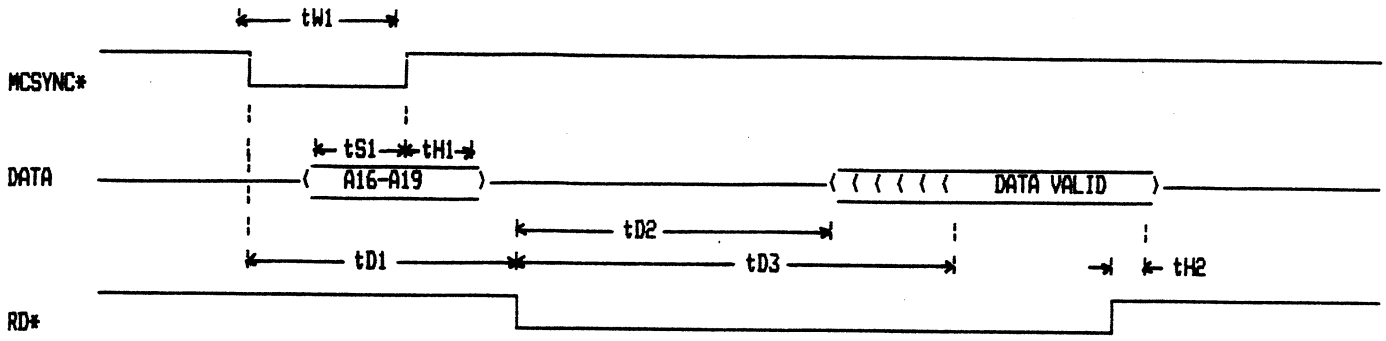
SYMBOL	PARAMETER	MIN	MAX
tD1	Delay from CLOCK* to MCSYNC* low	-10	
tD2	Delay from MCSYNC* to MCSYNC* and CLOCK* high	60	
tD3	Delay from CLOCK* to valid Data (2)(4)		35
tD4	Delay from MCSYNC* and CLOCK* high to WR*	-50	
tD5	Delay from CLOCK* to WR* high	160	
tH1	Address 16-19 hold after MCSYNC*	17	
tH2	Data hold after CLOCK* (3)(4)	205	
tH3	Data hold after WR* (3)(4)	150	
tS1	Address 16-19 setup to MCSYNC* low	10	
tS2	Address 16-19 setup to MCSYNC* and CLOCK* high	60	
tS3	Data setup to WR* (2)(4)	30	
tS4	Address 0-15 setup to MCSYNC* and CLOCK* high	30	
tS5	MEMRQ* setup to MCSYNC* and CLOCK* high	25	
tW1	CLOCK* width	199	6000
tW2	CLOCK* high width	50	
tW3	CLOCK* low width	50	
tW4	MCSYNC* pulse width	35	
tW5	WR* pulse width (4)	85	

All times given in nanoseconds.

Notes:

1. Write access starts with clock going low in T2 regardless of WR*. Access will not complete until after WR*.
2. The worst case setup time for data is based on tD3 or tS3 depending on WR*.
3. The worst case hold time for data is based on tH2 or tH3 depending on WR*
4. Typically, tD3, tD5 and tH2 are used for advanced writes while tS3, tH3 and tW5 are used for normal writes.
5. Valid address 0-15 and MEMRQ* are to be held for the minimum data hold time or longer.

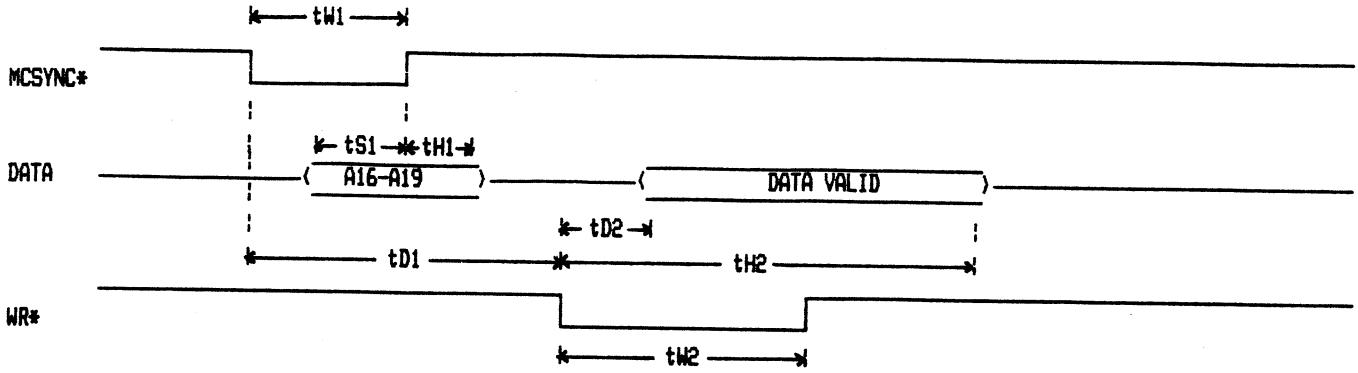
Figure 2-8B. DMA Write Timing (7712)



SYMBOL	PARAMETER	MIN	MAX
tD1	Delay from MCSYNC* low to RD*	70	
tD2	Delay from RD* to Data driven on BUS	15	50
tD3	Delay from RD* to Valid Data (tAR)		300
tH1	Address 16-19 hold after MCSYNC*	17	
tH2	Data hold after RD*	15	50
tS1	Address 16-19 setup to MCSYNC*	10	
tW1	MCSYNC* pulse width	35	

All times given in nanoseconds.

Figure 2-9A. Unclocked DMA Read Timing (7712)
(STATUS1* and CLOCK* are not active)



SYMBOL	PARAMETER	MIN	MAX
tD1	Delay from MCSYNC* low to WR*	70	
tD2	Delay from WR* to valid Data	40	
tH1	Address 16-19 hold after MCSYNC*	17	
tH2	Valid Data hold after WR*	245	
tS1	Address 16-19 setup to MCSYNC*	10	
tW1	MCSYNC* pulse width	35	
tW2	WR* pulse width	55	

All times given in nanoseconds.

Figure 2-9B. Unclocked DMA Write Timing (7712)
(CLOCK* is not active)